ABSTRACT

A technique for reducing leakage current in static CMOS devices by adding additional transistors in series between selected inverters or logic gates and ground or power. NMOS and PMOS transistors are added to selected buffers comprised of two inverters in series. The PMOS transistor is connected between the first inverter and power and the NMOS transistor is connected between the second inverter and ground. The added transistors are controlled by a memory cell to be on when the buffer is being used and off when the buffer is unused. Alternatively, no PMOS transistor is added and an existing PMOS transistor of the first inverter is manufactured to sit in a V_{gg} well. The same techniques are employed with selected buffer pairs and logic gates.